μPD78C05A/06A
HIGH-END, 8-BIT, SINGLE-CHIP CMOS MICROCOMPUTERS

Description

The μPD78C05A and μPD78C06A are advanced CMOS 8-bit general purpose, single-chip microcomputers intended for applications requiring 8-bit microprocessor control and extremely low power consumption. They are ideally suited for portable, battery-powered/backed-up products. Subsets of the μPD7801, the μPD78C05A/06A integrate an 8-bit ALU, 4K-byte ROM, 128-byte RAM, 46 I/O lines, an 8-bit timer, and a serial I/O port on a single die. Expanded system operation can easily be implemented using industry standard peripheral and memory components. Total memory space can be increased to 64K bytes.

The μPD78C05A/06A lend themselves well to low-power, portable applications by featuring two power-down modes to further conserve power when the processor is not active. The μPD78C06A is packaged in a 64-pin plastic miniflat package. The μPD78C05A is a ROM-less version, packaged in a 64-pin QUIP, and designed for prototype development and small volume production.

Features

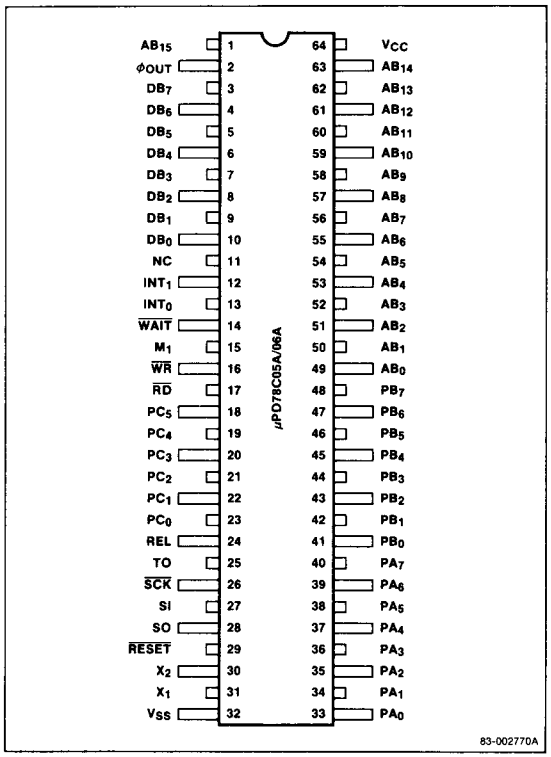
- ☐ CMOS silicon gate technology; +5 V supply
- ☐ Complete single-chip microcomputer
  - —8-bit ALU
  - —4K-byte ROM
  - —128-byte RAM
- ☐ 6.25 MHz
- ☐ Low power consumption
- ☐ 46 I/O lines
- ☐ Expansion capabilities
  - —60K-byte external memory address range
  - —8080A bus compatible
- ☐ Serial I/O port
- ☐ 101 instructions with multiple address modes
- ☐ Power-down modes
  - —Halt mode
  - —Stop mode
- ☐ 8-bit timer
- ☐ Prioritized interrupt structure
  - —Two external
  - —One internal
- ☐ On-chip clock generator
- ☐ ROM-less version available (78C05A)

Ordering Information

Part Number	Package Type
μPD78C05AG-36	64-pin plastic QUIP
μPD78C06AG-12	64-pin plastic miniflat

Pin Configurations

64-Pin Plastic QUIP



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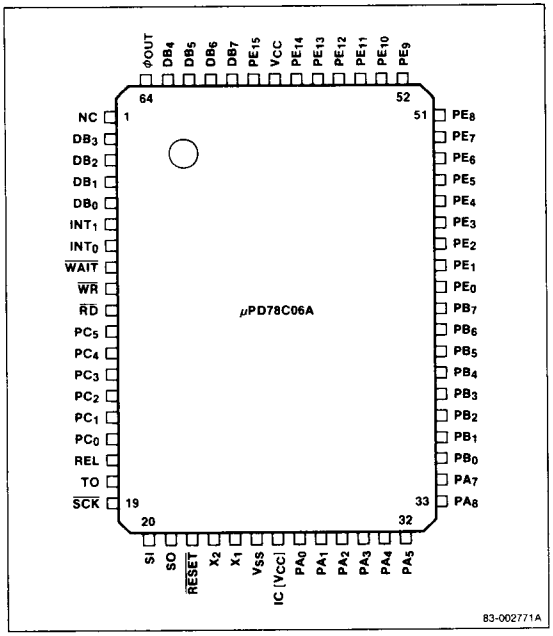
Pin Configurations (cont)

64-Pin Plastic Miniflat



Pin Identification

Plastic QUIP

No.	Symbol	Function
1	PE_{15} (78C06A) AB_{15}(78C05A)	Address bus/output port E, bit 15 Address bus, bit 15
2	ϕ_{OUT}	Clock output
3-10	DB_7-DB_0	Bidirectional data bus
11	NC	Not connected
12, 13	INT_1, INT_0	Interrupt inputs 1 and 0
14	$\overline{WAIT}$	Wait request input
15	M_1	Machine cycle 1 output
16	$\overline{WR}$	Write strobe output
17	$\overline{RD}$	Read strobe output
18-23	PC_5-PC_0	Input port C
24	REL	STOP release input
25	TO	Timer output
26	$\overline{SCK}$	Serial clock input/output

Plastic QUIP (cont.)

No.	Symbol	Function
27	SI	Serial data input
28	SO	Serial data output
29	$\overline{RESET}$	Reset input
30, 31	X_2, X_1	Crystal connections
32	V_{SS}	Ground potential
33-40	PA_0-PA_7	I/O port A, bits 0-7
41-48	PB_0-PB_7	I/O port B, bits 0-7
49-63	PE_0-PE_{14} (78C06A) AB_0-AB_{14} (78C05A)	Address bus/output port E, bits 0-14 Address bus, bits 0-14
64	V_{CC}	Power supply

Plastic Miniflat

No.	Symbol	Function
1	NC	Not connected
2-5	DB_3-DB_0	Bidirectional data bus, bits 3-0
6, 7	INT_1, INT_0	Interrupt inputs 1 and 0
8	$\overline{WAIT}$	Wait request input
9	$\overline{WR}$	Write strobe output
10	$\overline{RD}$	Read strobe output
11-16	PC_5-PC_0	Input port C
17	REL	STOP release input
18	TO	Timer output
19	$\overline{SCK}$	Serial clock input/output
20	SI	Serial data input
21	SO	Serial data output
22	$\overline{RESET}$	Reset input
23, 24	X_2, X_1	Crystal connections
25	V_{SS}	Ground potential
26	IC (V_{CC})	Internally conected to V_{CC}
27-34	PA_0-PA_7	I/O port A, bits 0-7
35-42	PB_0-PB_7	I/O port B, bits 0-7
43-57	PE_0-PE_{14}	Address bus/output port E, bits 0-14
58	V_{CC}	Power supply
59	PE_{15}	Address bus/output port E, bit 15
60-63	DB_7-DB_4	Bidirectional data bus, bits 7-4
64	ϕ_{OUT}	Clock output

Pin Functions

DB_0-DB_7 [Data Bus]

The 8-bit bidirectional data bus transfers data between the accumulator and external memory or memory-mapped I/O.

INT_0, INT_1 [Interrupts 0 and 1]

INT_0 is a rising-edge-triggered external interrupt input. INT_1 is an active-high external interrupt input. Both inputs must be held high for a least 2 μs to be recognized as valid.

$\overline{WAIT}$ [Wait Request]

The $\overline{WAIT}$ input is used to interface with slow memories or peripherals. $\overline{WAIT}$ is sampled at the end of machine cycle T_2. If it is low, then the processor goes into a wait state until $\overline{WAIT}$ returns high.

M_1 [Machine Cycle 1]

(78C05A only) The M_1 output is high during machine cycles T_1 through T_3 of the first opcode fetch of an instruction.

$\overline{WR}$ [Write Strobe]

When the $\overline{WR}$ output is low, valid output data is available on the data bus.

$\overline{RD}$ [Read Strobe]

The processor loads data from the data bus into the accumulator on the rising edge of the $\overline{RD}$ output.

PC_0-PC_5 [Port C]

The 6-bit input port has internal pull-up resistors. When contents of the port buffer are transferred to the accumulator, they fill the least significant six bits.

REL [STOP Release]

The STOP release input has an internal pull-down resistor. High level on REL releases the processor from stop mode, allowing the clock generator to restart.

TO [Timer Output]

Frequency of square wave output at TO is determined by the timer register contents. TO outputs a low level after reset.

$\overline{SCK}$ [Serial Clock]

The control clock for the serial data port is user-programmable as an input or output.

SI [Serial Data Input]

The SI input loads into the serial register on the rising edge of SCK.

SO [Serial Data Output]

On the falling edge of SCK, the serial register outputs data to SO, most significant bit first.

$\overline{RESET}$ [Reset]

A low level on $\overline{RESET}$ input of more than 8 μs resets the processor.

X_1, X_2 [Crystal Connections]

These pins connect to the internal clock generator circuit. If an external clock generator is used, then it is connected to X_1.

V_{SS} [Ground]

This is the power supply ground potential input.

IC [V_{CC}]

(78C06A only) This is the internal connection to V_{CC} through a high impedance. It should be left open.

PA_0-PA_7 [Port A]

Port A is an 8-bit latched output port. Data can be readily transferred between the accumulator and the output latch buffers. The contents of the output latches can be modified using arithmetic and logic instructions. Data remains latched at port A unless it is acted on by another port A instruction or a RESET is issued.

PB_0-PB_7 [Port B]

Port B is an 8-bit I/O port. Data is latched at port B in both the input and output modes. Each bit of port B can be independently set to either input or output mode. The mode B register programs the individual lines of port B to be either an input (mode $B_n = 1$) or an output (mode $B_n = 0$).

PE_0-PE_{15} [Port E]

(78C06A only) Port E is a 16-bit address bus/output port. It can be set to one of two operating modes using the PER or PEX instruction.

- 16-bit address bus: the PER instruction sets this mode for use with external I/O or memory expansion (up to 60K bytes, externally).
- 16-bit output port: the PEX instruction sets port E to a 16-bit output port. The contents of B and C registers appear on PE_8-PE_{15} and PE_0-PE_7, respectively.

AB_0-AB_{15} [Address Bus]

These lines are the 16-bit address bus to the main memory. The 78C05A, having no internal ROM, must address the area from 0 to 4096 as external ROM.

The 78C05A AB lines are unlike the 78C06A PE lines in that they have no internal latches. When the Port E output instruction PEX is executed in a 78C05A, the register pair BC is output to the AB lines for only one clock cycle during the third machine cycle. This is provided to allow external hardware to emulate the Port E operation of the 78C06A.

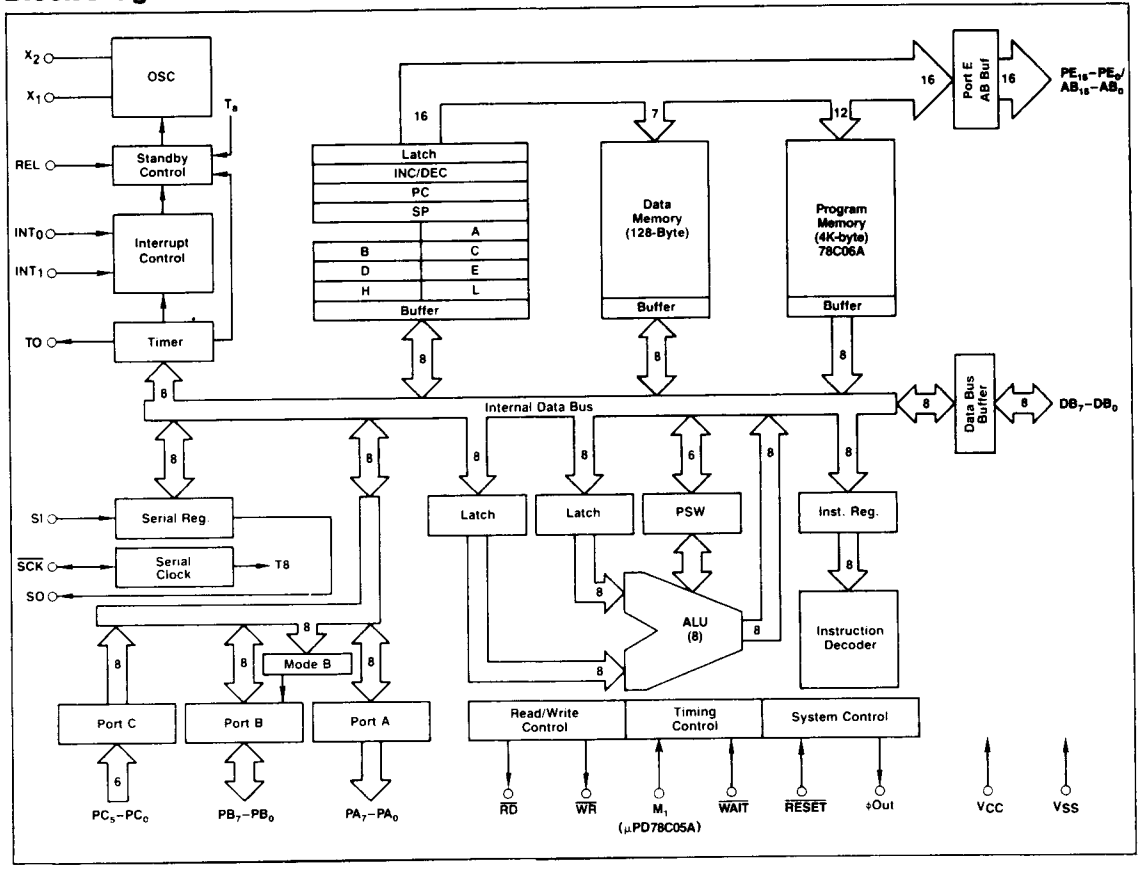
V_{CC} [Power Supply]

This pin is the power supply input, 3.5 to 6.0 V during normal operation.

ϕ OUT [Clock Output]

The system clock frequency, which is 1/4 or 1/8 of the crystal frequency, is output on this pin. ϕ OUT is active in halt mode but is held high in stop mode.

Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{CC} + 0.3 V
Output voltage, V_O	−0.3 V to V_{CC} + 0.3 V
Output high current, I_{OH} (device total)	−5 mA
Output low current, I_{OL} (device total)	43.5 mA
Operating temperature, T_{OPR}	−40 to +85 °C
Storage temperature, T_{STG}	−65 to +150 °C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = +25 °C; V_{CC} = GND = 0 V

		Limits				Test
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input capacitance	C_I			15	pF	f_c = 1 MHz; unmeasured pins returned to 0 V
Output capacitance	C_O			15	pF	
I/O capacitance	$C_{I/O}$			15	pF	

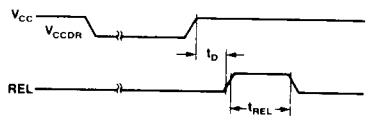
Low-Power Data Memory Retention in Stop Mode

T_A = −40 to + 85 °C

		Limits				Test
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Data retention voltage	V_{CCDR}	2.0			V	
Data retention supply current	I_{CCDR}		0.8	20	μA	V_{CCDR} = 2.0 V, (X_1 = 0 V, X_2 = open)
Data retention input low RESET voltage	V_{ILDR}	0		0.2 V_{CCDR}		
Data retention input high RESET voltage	V_{IHDR}	0.8 V_{CCDR}		V_{CCDR}	V	
REL input delay time	t_D	500			μs	
REL input high time	t_{REL}	10			μs	

Note:

(1) In data retention mode, input voltages to $\overline{WAIT}$ and PC_0-PC_5 pins (with pull-up resistors) should be maintained the same as V_{CCDR} level; other input voltages should be kept less than V_{CCDR} level.



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DC Characteristics

$T_A = -40$ to $+85°C$; $V_{CC} = +5\ V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input high voltage	V_{IH1}	0.7 V_{CC}		V_{CC}	V	$\overline{INT_0}$, $\overline{INT_1}$, $\overline{WAIT}$, PB_0-PB_7, PC_0-PC_5
	V_{IH2}	0.75 V_{CC}			V	$\overline{RESET}$, $\overline{SCK}$, REL, SI
	V_{IH3}	$V_{CC} - 2.0$		V_{CC}	V	DB_0-DB_7
	V_{IH4}	$V_{CC} - 0.5$		V_{CC}	V	X_1
Input low voltage	V_{IL1}	0		0.3 V_{CC}	V	$\overline{INT_0}$-$\overline{INT_1}$, $\overline{WAIT}$, PB_0-PB_7, PC_0-PC_5
	V_{IL2}	0		0.25 V_{CC}	V	$\overline{RESET}$, $\overline{SCK}$, REL, SI
	V_{IL3}	0		0.8	V	DB_0-DB_7
	V_{IL4}	0		0.5	V	X_1
Output high voltage	V_{OH1}	2.4			V	$I_{OH} = -100\ \mu A$
	V_{OH2}	$V_{CC}-0.5$			V	$I_{OH} = -50\ \mu A$
Output low voltage	V_{OL}			0.45	V	$I_{OL} = 1.8$ mA
Input high current	I_{IH1}	7		100	μA	$V_{IN} = V_{CC}$ (REL)
	I_{IH2}			45	μA	$V_{IN} = V_{CC}$ (X_1)
Input low current	I_{IL1}	−7		−100	μA	$V_{IN} = 0$ V (WAIT, PC_0-PC_5)
	I_{IL2}			−45	μA	$V_{IN} = 0$ V (X_1)
Input high leakage current	I_{LIH}			3.2	μA	$V_{IN} = V_{CC}$ (except REL, X_1)
Input low leakage current	I_{LIL1}			−3.2	μA	$V_{IN} = 0$ V (except WAIT, PC_0-PC_5, X_1)
	I_{LIL2}			−3.2	μA	$V_{IN} = 0$ V (Stop mode, X_1)
Output high leakage current	I_{LOH}			3.2	μA	$V_{OUT} = V_{CC}$
Output low leakage current	I_{LOL}			−3.2	μA	$V_{OUT} = 0$ V
V_{CC} supply current	I_{CC1}		4	7.5	mA	Operation mode
	I_{CC2}		1.2	2.7	mA	Halt mode
	I_{CC3}		1	20	μA	Stop mode ($X_1 = 0$ V, X_2 = Open)

AC Characteristics

Read/Write Operation

78C05A, $t_{CY\phi} = 660$ ns; 78C06A, $t_{CY\phi} = 1320$ ns

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{RD}$ low time	t_{RR}	1070 + 660			ns	
$\overline{RD}$ LE to $\overline{WAIT}$ LE	t_{RWT}			460	ns	
Address (PE_0-PE_{15}) to $\overline{WAIT}$ LE	t_{AWTI}			790	ns	
$\overline{WAIT}$ set-up time to ϕ_{OUT} LE↓	t_{WTS}	370			ns	
$\overline{WAIT}$ hold time after ϕ_{OUT} LE	t_{WTH}	0			ns	
M_1 to $\overline{RD}$ LE (1)	t_{MR}	108			ns	
$\overline{RD}$ TE to M_1 (1)	t_{RM}	130			ns	
ϕ_{OUT} LE to $\overline{WR}$ LE	$t_{\phi W}$			175	ns	
Address (PE_0-PE_{15}) to ϕ_{OUT} TE	$t_{A\phi}$	420			ns	
Address (PE_0-PE_{15}) to ϕ_{OUT} TE (1)	$t_{A\phi}$-	90			ns	
Address (PE_0-PE_{15}) to data output	t_{AD2}	510			ns	
Data output to $\overline{WR}$ TE	t_{DW}	740 + 660N			ns	
$\overline{WR}$ TE to data stable time	t_{WD}	130			ns	
Address (PE_0-PE_{15}) to $\overline{WR}$ LE	t_{AW}	460			ns	
$\overline{WR}$ TE to address stable time	t_{WA}	180			ns	
$\overline{WR}$ low time	t_{WW}	690 + 900N			ns	
$\overline{WR}$ LE to $\overline{WAIT}$ LE	t_{WWT}			110	ns	

Note:

(1) Applies only to 78C05A.

(2) N is number of WAIT states (T_{WAIT}).
In the 78C06A, two WAIT states are automatically inserted when accessing internal ROM.

(3) LE is leading edge and TE is trailing edge.

AC Characteristics (cont)

Bus Timing Depending on $t_{CY\phi}$

$T_A = -40$ to $+85°C$

Symbol	Formula	Min/Max	Unit
$t_{R\phi}$	$(1/2)T - 150$	Min	ns
t_{AD1}	$(3/2 + N)T - 200$	Max	ns
$t_{RA}(T3)$	$(1/2)T - 150$	Min	ns
$t_{RA}(T4)$	$(3/2)T - 150$	Min	ns
t_{RD}	$(1 + N)T - 200$	Max	ns
t_{RR}	$(2 + N)T - 250$	Min	ns
t_{RWT}	$T - 200$	Max	ns
t_{AWTI}	$(3/2)T - 200$	Max	ns
t_{WTS}	$(1/3)T + 150$	Min	ns
t_{MR} (1)	$(3/8)T - 140$	Min	ns
t_{RM} (1)	$(1/2)T - 200$	Min	ns
$t_{A\phi}$ (1)	$(1/2)T - 240$	Min	ns
$t_{A\phi}$	$T - 240$	Min	ns
t_{AD2}	$T - 150$	Min	ns
t_{DW}	$(3/2 + N)T - 250$	Min	ns
t_{WD}	$(1/2)T - 200$	Min	ns
t_{AW}	$T - 200$	Min	ns
t_{WA}	$(1/2)T - 150$	Min	ns
t_{WW}	$(3/2 + N)T - 300$	Min	ns
t_{WWT}	$(1/2)T - 220$	Max	ns
t_{CYK}	$2T$	Min	ns
t_{KKL}	$T - 120$	Min	ns
t_{KKH}	$T - 120$	Min	ns

Note:

(1) For 78C05A only

(2) N = Number of T_{WAIT} states
In the 78C06A, two wait states are automatically inserted when accessing internal ROM.
$T = t_{CY\phi}$ for 78005A
$T = 2t_{CY\phi}$ for 78C06A
t_{CY} assumes 50% duty cycle on X_1.

Serial Operation

78C05A, $t_{CY\phi} = 660$ ns; 78C06A, $t_{CY\phi} = 1320$ ns

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{SCK}$ cycle time	t_{CYK}	1270 1280		80,000	ns ns	$\overline{SCK}$ input $\overline{SCK}$ output
$\overline{SCK}$ low time	t_{KKL}	515 520			ns ns	$\overline{SCK}$ input $\overline{SCK}$ output
$\overline{SCK}$ high time	t_{KKH}	515 520			ns ns	$\overline{SCK}$ input $\overline{SCK}$ output
SI set-up time to $\overline{SCK}$ TE	t_{SIS}	200			ns	
SI hold time after $\overline{SCK}$ TE	t_{SIH}	250			ns	
$\overline{SCK}$ LE to SO delay time	t_{KO}			300	ns	

Note:

(1) Input timings are measured at V_{IH} min and V_{IL} max.

(2) Output timings are measured at $V_{OH} = 2.4$ V, $V_{OL} = 0.45$ V, and load = one TTL + 200 pF.

(3) LE is leading edge and TE is trailing edge.

Clock Timing

$T_A = -40$ to $+85°C$ $V_{DD} = +5$ V $\pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
X_1 input cycle time	t_{CYX}	160		10,000	ns	
X_1 input low time	t_{XXL}	75			ns	
X_1 input high time	t_{XXH}	75			ns	
ϕ_{OUT} cycle time (2)	$t_{CY\phi}$	1,280		80,000	ns	
ϕ_{OUT} low time (2)	$t_{\phi\phi L}$	515			ns	
ϕ_{OUT} high time (2)	$t_{\phi\phi H}$	515			ns	
ϕ_{OUT} cycle time (1)	$t_{CY\phi}$	640		40,000	ns	
ϕ_{OUT} Low time (1)	$t_{\phi\phi L}$	195			ns	
ϕ_{OUT} high time (1)	$t_{\phi\phi H}$	195			ns	
ϕ_{OUT} rise/ fall time	t_R, t_F			120	ns	

Note:

(1) Applies only to 78C05A. ($t_{CY\phi} = 4/f_{OSC}$)

(2) Applies only to 78C06A. ($t_{CY\phi} = 8/f_{OSC}$)

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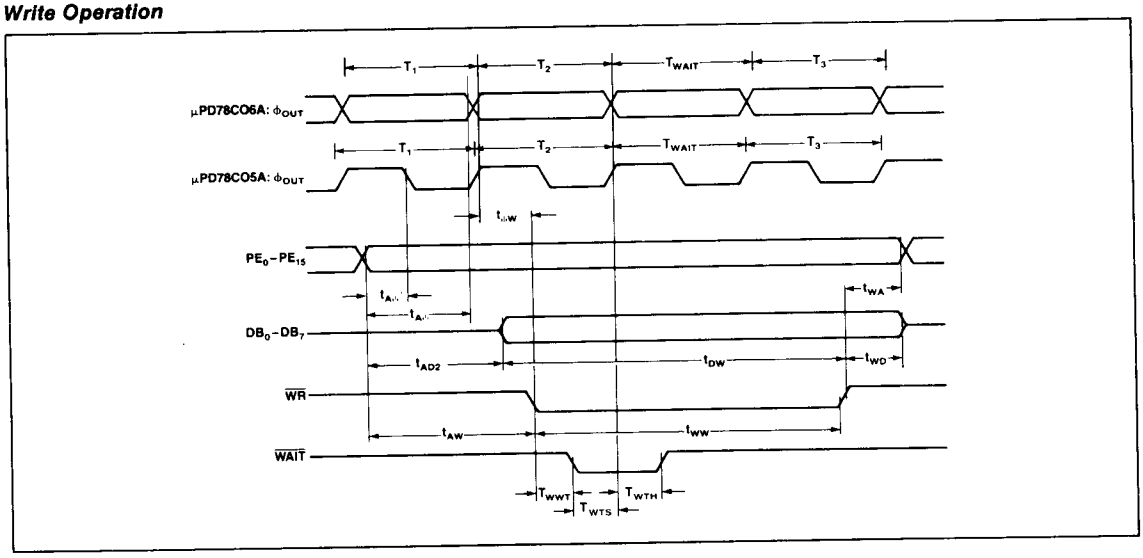
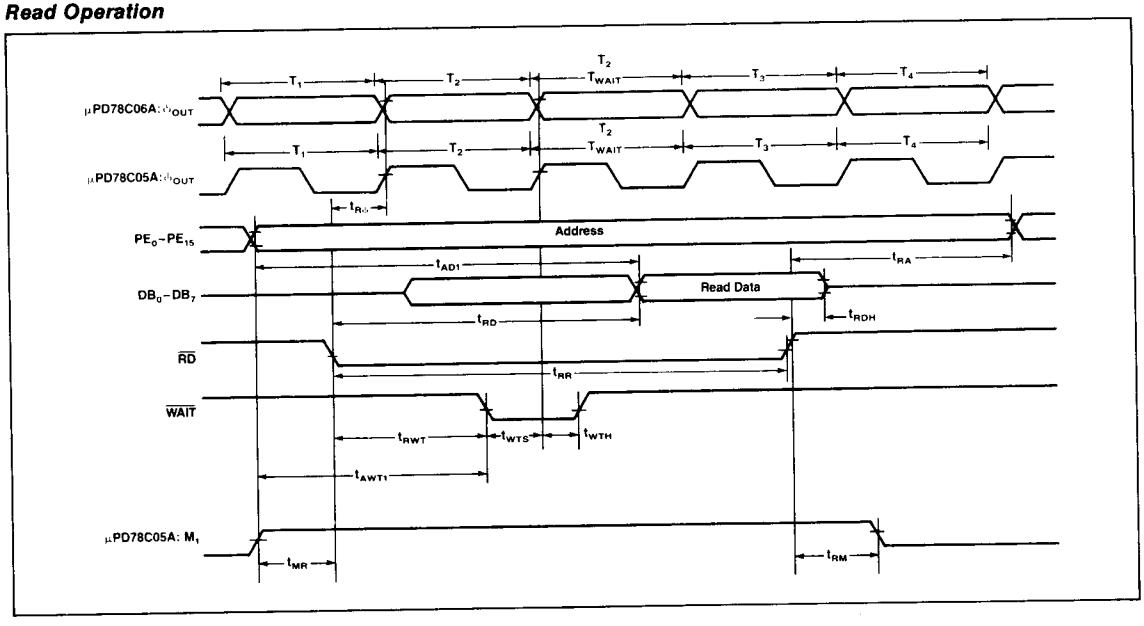
Timing Waveforms

Write Operation

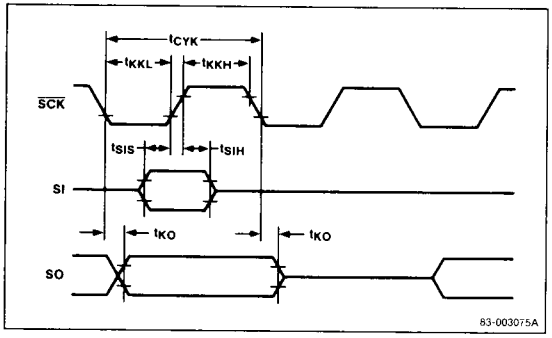


Read Operation

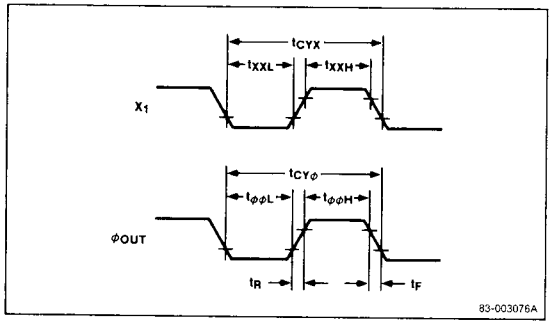


Timing Waveforms (cont)

Serial Operation



Clock Timing



Functional Description

Memory Map

The μPD78C06A can directly address up to 64K bytes of memory. Except for the on-chip ROM (0-4,095) and RAM (65,408-65,535), any memory location can be used as either ROM or RAM. Figure 1 defines the 0-64K-byte memory space for the μPD78C06A showing that the reset start address, interrupt start address, call tables, etc, are located in the internal ROM area.

Timer Operation

A programmable 8-bit timer (figure 2) is provided on-chip for measuring time intervals, generating pulses, and general time-related control functions. It is capable of measuring time intervals from 5 μs to 21 ms in duration. The timer consists of a prescaler that decrements an 8-bit counter at a fixed 5-μs or 82-μs rate.

Countup operation is initiated upon execution of the STM instruction. When the contents of the upcounter are incremented and a coincidence with the Timer Reg. occurs, an internal interrupt (INT_T) is generated. The duration of the time-out may be altered by loading new contents into the timer register.

The timer flip-flop is set by the STM instruction and reset on a countup operation. Its output (TO) is available externally and may be used for general external synchronization.

Serial Port Operation

The on-chip serial port (figure 3) provides basic synchronous serial communication functions allowing the μPD78C05A/06A to serially interface with external devices.

Serial transfers are synchronized with either the internal clock or an external clock input ($\overline{SCK}$). The transfer rate is fixed at $f_{OSC}/8$ if the internal clock is used or is variable between dc and $f_{OSC}/8$ when an external clock is used. The clock source select is determined by the serial mode register. Data on the SI (serial input) line is latched into the serial register on each rising edge of the serial clock ($\overline{SCK}$). Concurrently, data is transferred out of the serial register onto the SO (serial output) line with each falling edge of $\overline{SCK}$. At this time, receive and transmit operations through the SI/SO port are enabled. Receive and transmit operations are performed MSB first.

Interrupt Structure

The μPD78C05A/06A provide a maskable interrupt structure capable of handling vectored prioritized interrupts. Interrupts can be generated from three different sources: two external interrupts and a timer interrupt. When activated, each interrupt branches to a designated memory vector location for that interrupt. See table 1.

Table 1. Interrupt Structure

INT	Vectored Memory Location	Priority	Type
INT_T	8	2	Internal, timer overflow
INT_0	4	1	External, level sensitive
INT_1	16	3	External, rising-edge sensitive

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Figure 1. Memory Map

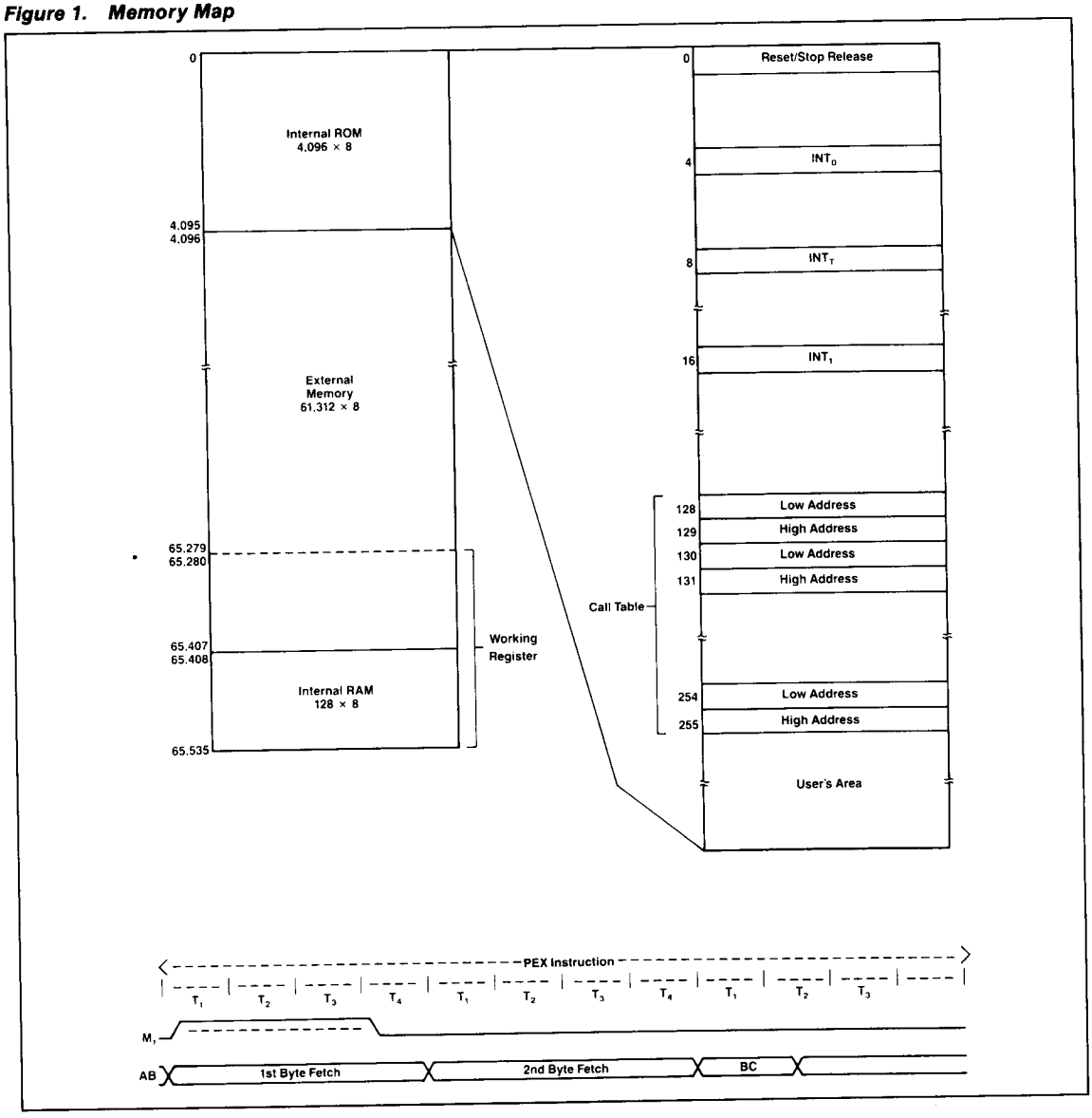


Figure 2. Timer Block Diagram

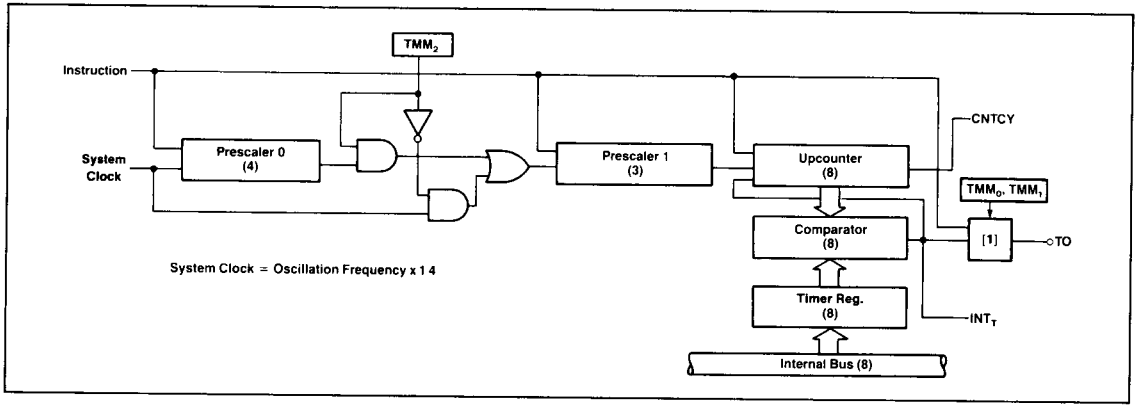
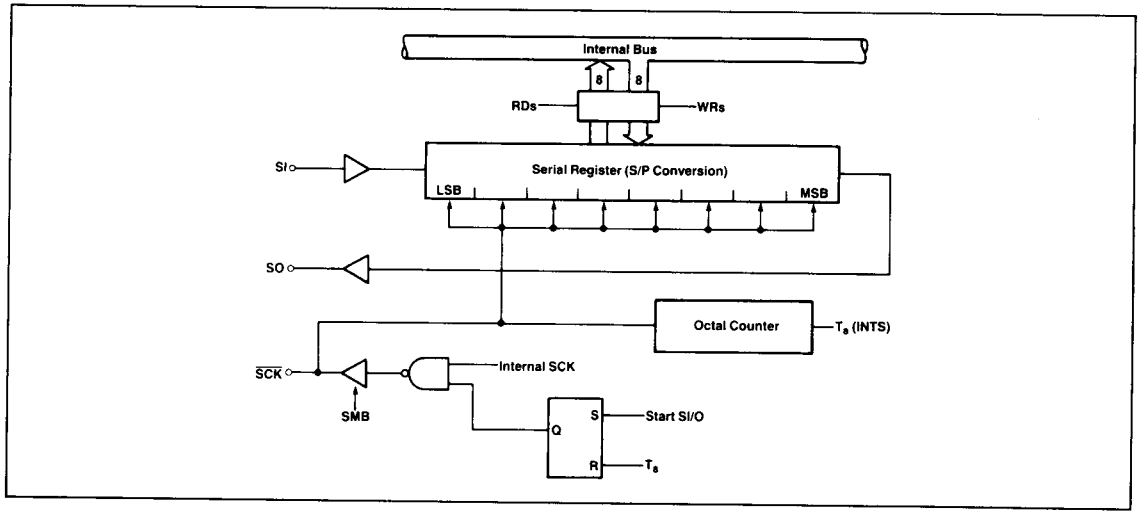


Figure 3. Serial Port Diagram



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Reset

An active-low signal on the $\overline{RESET}$ input for more than 4 μs forces the μPD78C05A/06A into a reset condition, which affects the following internal functions:

- The interrupt enable flags are reset, and interrupts are inhibited.
- The interrupt request flag is reset.
- The halt flip-flop is reset, and the halt state is released.
- The contents of the mode B register are set to FFH, and port B becomes an input port.
- All flags are reset to 0.
- The internal count register for timer operation is set to FFH and the timer F/F is reset.
- The contents of the program counter are set to 0000H.
- Data bus (DB_0-DB_7), $\overline{RD}$, and $\overline{WR}$ go to a high-impedance state.

Once the $\overline{RESET}$ input goes high, the program is started at location 0000H.

Stop and Halt Modes

The μPD78C05A/06A have a stop and a halt mode. The effects of stop and halt on various functions are shown in table 2.

Registers

The μPD78C05A/06A contain seven 8-bit registers and two 16-bit registers. See figure 4.

General Purpose Registers

The general purpose registers B, C, D, E, H, L can function as auxiliary registers to the accumulator or in pairs as data pointers (BC, DE, HL). Automatic increment and decrement addressing mode capabilities extend the uses for the DE and HL register pairs.

Figure 4. Registers

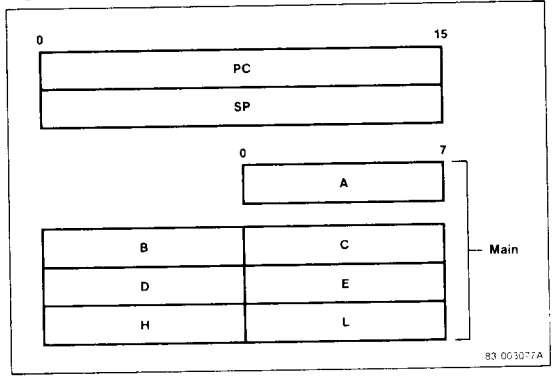


Table 2. Halt and Stop Modes

Function	Halt Mode	Stop Mode
Oscillator	Run	Stop
Internal system clock	Stop	
Timer	Run	
Timer register	Hold	Set
Upcounter, prescaler 0, 1	Run	Cleared
Serial interface	Run	Run (1)
Serial clock	Hold	Hold
Interrupt control circuit	Run	Stop
Interrupt enable flag	Hold	Reset
INT_0, INT_1 input	Active	Inactive
INT_T		—
T_8 (INTFS)		—
Mask register	Hold	Set
Pending interrupts (INTFX)		Reset
REL input	Inactive	Active
RESET input	Active	
On-chip RAM	Hold	Hold
Output latch in ports A, B, E		
Program counter (PC)		Cleared
Stack pointer (SP)		Unknown
General registers (A, B, C, D, E, F, L)		
Program status word (PSW)		Reset
Mode B register		Hold
Standby control register (SC_0-SC_3)		
Standby control register (SC_4)		Set
Timer mode register (TMM_0-TMM_1)		Hold
Timer mode register (TMM_1)		Set
Serial mode register (SM)		Hold
Data bus (DB_0-DB_7)	High-Z	High-Z
RD, WR output	High	High

Note:

(1) Serial clock counter is running and T_8 is generated; however, there are no effects from it.

Accumulator [A]

All data transfers between the μPD78C05A/ 06A and external memory or I/O are done through the accumulator.

Program Counter [PC]

The PC is a 16-bit register containing the address of the next instruction to be fetched. Under normal program flow, the PC is automatically incremented. However, in the case of a branch instruction, the PC contents are from another register or an instruction's immediate data. A reset sets the PC to 0000H.

Stack Pointer [SP]

The stack pointer is a 16-bit register used to maintain the top of the stack area (last-in/first-out). The contents of the SP are decremented during a Call or Push instruction or if an interrupt occurs. The SP is incremented during a Return or POP instruction.

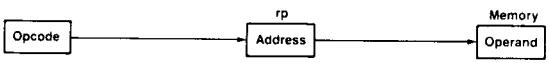
Address Modes

Register Addressing

The instruction opcode specifies a register that contains the operand.

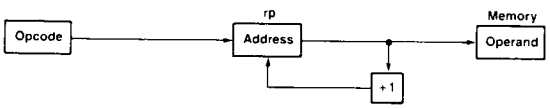
Register Indirect Addressing

The instruction opcode specifies a register pair that contains the memory address of the operand. Mnemonics with an X suffix indicate this address mode.

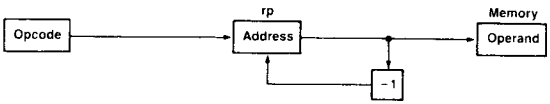


Automatic Increment Addressing

The opcode specifies a register pair that contains the memory address of the operand. The contents of the register pair are automatically incremented to point to a new operand. This mode provides automatic sequential stepping when working with a table of operands.

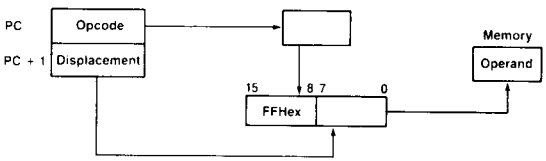


Automatic Decrement Addressing



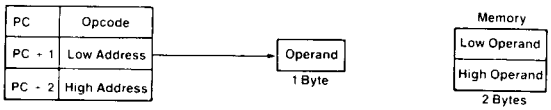
Working-Register Addressing

The contents of the register are linked with the byte following the opcode to form a memory address that contains the operand. The V register is used to indicate the memory page. This address mode is useful as a short-offset address mode when working with operands in a common memory page where only one additional byte is required for the address. Mnemonics with a W suffix indicate this address mode. In the μPD78C05A/ 06A, the V register is always FFH.



Direct Addressing

The two bytes following the opcode specify an address of a location containing the operand.

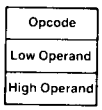


Immediate Addressing

PC
PC + 1

Immediate Extended Addressing

PC
PC + 1
PC + 2



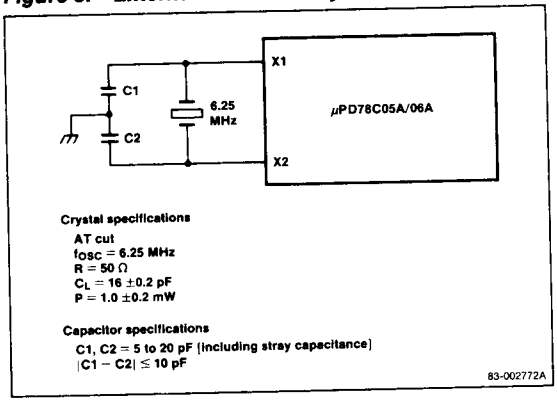
4

Clock Driver Circuit

The 6.25-MHz master timing signal is from an external oscillator connected to pin X1 or from an internal oscillator controlled by an external 6.25-MHz crystal connected to pins X1 and X2 (figure 5). Dividing f_{OSC} by four creates the internal CPU clock (f_{ϕ} = 1.5625 MHz).

A system clock is available for external use at the ϕ_{OUT} pin. Its frequency is 1.5625 MHz (6.25/4) or 0.78125 MHz (6.25/8) for 78C05A and 78C06A, respectively.

Figure 5. External 6.25-MHz Crystal



Instructions

Instruction Set Definitions

Operand	Description
r	A, B, C, D, E, H, L
r1	B, C, D, E, H, L
r2	A, B, C
sr	PA, PB, PC, MK, MB, TM_0, TM_1, S, SM, SC
sr1	PA, PB, PC, MK, S, TM_0, TM_1, SC
sr2	PA, PB, PC, MK
rp	SP, B, D, H
rp1	B, D, H
rpa	B, D, H, D^+, H^+, D^-, H^-
wa	8-bit immediate data used to access working register area
word	16-bit immediate data
byte	8-bit immediate data
bit	1-bit immediate data
if	F0, F1, FT, FS
F	CY, Z
fa	10-bit immediate data used to access fixed area in locations 0-2047
ta	5-bit immediate data used to access table in locations 128-191
n	Number of bytes in an instruction

Note:

(1) When special register operands sr, sr1, sr2 are used, PA = port A, PB = port B, PC = port C, MK = mask register, MB = mode B register, SM = serial mode register, SC = standby control register, TM_0 = timer register 0, TM_1 = timer register 1, S = serial register.

(2) When register pair operands rp, rp1 are used, SP = stack pointer, B = BC, D = DE, H = HL.

(3) Operands rpa, rp1, wa are used in indirect addressing and auto-increment/auto-decrement addressing modes. B = (BC), D = (DE), H = (HL), D^+ = $(DE)^+$, H^+ = $(HL)^+$, D^- = $(DE)^-$, and H^- = $(HL)^-$.

(4) When the interrupt operand "if" is used, F0 = INTF0, F1 = INTF1, FT = INTFT, FS = INTFS.

(5) When the operand F is used, CY = Carry and Z = Zero.

(6) The V register is always FFH.

Instruction Set

Mnemonic	Operand	Bytes	*Clocks	Operation	Skip Condition	Flags CY	Flags Z
8-Bit Data Transfer							
MOV	r1,A	1	4/6	(r1) ← (A)			
MOV	A,r1	1	4/6	(A) ← (r1)			
MOV	sr,A	2	10/14	(sr) ← (A)			
MOV	A,sr1	2	10/14	(A) ← (sr1)			
MOV	r,word	4	17/25	(r) ← (word)			
MOV	word,r	4	17/25	(word) ← (r)			
MV1	r,byte	2	7/11	(r) ← (byte)			
STAW	wa	2	10/14	(FFH,wa) ← (A)			
LDAW	wa	2	10/14	(A) ← (FFH,wa)			
STAX	rpa	1	7/9	((rpa)) ← (A)			
LDAX	rpa	1	7/9	(A) ← ((rpa))			
16-Bit Data Transfer							
SBCD	word	4	20/28	(word) ← (C), (word + 1) ← (B)			
SDED	word	4	20/28	(word) ← (E), (word + 1) ← (D)			
SHLD	word	4	20/28	(word) ← (L), (word + 1) ← (H)			
SSPD	word	4	20/28	(word) ← (SP_L), ((word) + 1) ← (SP_H)			
LBCD	word	4	20/28	(C) ← (word), (B) ← (word + 1)			
LDED	word	4	20/28	(E) ← (word), (D) ← (word + 1)			
LHLD	word	4	20/28	(L) ← (word), (H) ← (word + 1)			
LSPD	word	4	20/28	(SP_1) ← (word)			
POP	rp1	2	14/18	($rp1_L$) ← ((SP)) ($rp1_H$) ← ((SP) + 1), (SP) ← (SP) + 2			
LXI	rp,word	3	10/16	(rp) ← word			
Arithmetic							
ADD	A,r	2	8/12	(A) ← (A) + (r)		↕	↕
ADDX	rpa	2	11/15	(A) ← (A) + ((rpa))		↕	↕
ADC	A,r	2	8/12	(A) ← (A) + (r) + (CY)		↕	↕
ADCX	rpa	2	11/15	(A) ← (A) + ((rpa)) + (CY)		↕	↕
SUB	A,r	2	8/12	(A) ← (A) − (r)		↕	↕
SUBX	rpa	2	11/15	(A) ← (A) − ((rpa))		↕	↕
SBB	A,r	2	8/12	(A) ← (A) − (r) − (CY)		↕	↕
SBBX	rpa	2	11/15	(A) ← (A) − ((rpa)) − (CY)		↕	↕
ADDNC	A,r	2	8/12	(A) ← (A) − (r)	No carry	↕	↕
ADDNCX	rpa	2	11/15	(A) ← (A) − ((rpa))	No carry	↕	↕
SUBNB	A,r	2	8/12	(A) ← (A) − (r)	No borrow	↕	↕
SUBNBX	rpa	2	11/15	(A) ← (A) − (rpa)	No borrow	↕	↕

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Instruction Set (cont)

Mnemonic	Operand	Bytes	*Clocks	Operation	Skip Condition	Flags CY	Flags Z
Logical							
ANA	A,r	2	8/12	(A) ← (A) ∧ (r)			↕
ANAX	rpa	2	11/15	(A) ← (A) ∧ ((rpa))			↕
ORA	A,r	2	8/12	(A) ← (A) ∨ (r)			↕
ORAX	rpa	2	11/15	(A) ← (A) ∨ ((rpa))			↕
XRA	A,r	2	8/12	(A) ← (A) ∨ (r)			↕
XRAX	rpa	2	12/15	(A) ← (A) ∨ ((rpa))			↕
GTA	A,r	2	8/12	(A) − (r) − 1	No borrow	↕	↕
GTAX	rpa	2	11/15	(A) − ((rpa)) − 1	No borrow	↕	↕
LTA	A,r	2	8/12	(A) − (r)	Borrow	↕	↕
LTAX	rpa	2	11/15	(A) − ((rpa))	Borrow	↕	↕
ONAX	rpa	2	8/12	(A) ∧ ((rpa))	No zero	↕	↕
OFFAX	rpa	2	11/15	(A) ∧ ((rpa))	Zero	↕	↕
NEA	A,r	2	8/12	(A) − (r)	No zero	↕	↕
NEAX	rpa	2	11/15	(A) − ((rpa))	No zero	↕	↕
EQA	A,r	2	8/12	(A) − (r)	Zero	↕	↕
EQAX	rpa	2	11/15	(A) − ((rpa))	Zero	↕	↕
Immediate Data Transfer (Accumulator)							
XRI	A,byte	2	7/11	(A) ← (A) ∨ byte			↕
ADINC	A,byte	2	7/11	(A) ← (A) − byte	No carry	↕	↕
SUINB	A,byte	2	7/11	(A) ← (A) − byte	No borrow	↕	↕
ADI	A,byte	2	7/11	(A) ← (A) + byte		↕	↕
ACI	A,byte	2	7/11	(A) ← (A) + byte + (CY)		↕	↕
SUI	A,byte	2	7/11	(A) ← (A) − byte		↕	↕
SBI	A,byte	2	7/11	(A) ← (A) − byte −(CY)		↕	↕
ANI	A,byte	2	7/11	(A) ← (A) ∧ byte			↕
ORI	A,byte	2	7/11	(A) ← (A) ∨ byte			↕
GTI	A,byte	2	7/11	(A) − byte − 1	No borrow	↕	↕
LTI	A,byte	2	7/11	(A) − byte	Borrow	↕	↕
ONI	A,byte	2	7/11	(A) ∧ byte	No zero	↕	↕
OFFI	A,byte	2	7/11	(A) ∧ byte	Zero		↕
NEI	A,byte	2	7/11	(A) − byte	No zero	↕	↕
EQI	A,byte	2	7/11	(A) − byte	Zero	↕	↕
Immediate Data Transfer (Special Register)							
ANI	sr2,byte	3	17/23	(sr2) ← (sr2) ∧ byte			↕
ORI	sr2,byte	3	17/23	(sr2) ← (sr2) ∨ byte			↕
OFFI	sr2,byte	3	14/20	(sr2) ∧ byte	Zero		↕
ONI	sr2,byte	3	14/20	(sr2) ∧ byte	No zero		↕

Instruction Set (cont)

Mnemonic	Operand	Bytes	*Clocks	Operation	Skip Condition	Flags CY	Flags Z
Working Register							
ANIW	wa,byte	3	16/22	(FFH, wa) ← (FFH, wa) ∧ byte			↕
ORIW	wa,byte	3	16/22	(FFH, wa) ← (FFH, wa) V byte			↕
GTIW	wa,byte	3	13/19	(FFH, wa) − byte − 1	No borrow	↕	↕
LTIW	wa,byte	3	13/19	(FFH, wa) − byte	Borrow	↕	↕
ONIW	wa,byte	3	13/19	(FFH, wa) ∧ byte	No zero		↕
OFFIW	wa,byte	3	13/19	(FFH, wa) ∧ byte	Zero		↕
NEIW	wa,byte	3	13/19	(FFH, wa) − byte	No zero	↕	↕
EQIW	wa,byte	3	13/19	(FFH, wa) − byte	Zero	↕	↕
Increment/Decrement							
INR	r2	1	4/6	(r2) ← (r2) + 1	Carry		↕
INRW	wa	2	13/17	(FFH, wa) ← (FFH, wa) + 1	Carry		↕
DCR	r2	1	4/6	(r2) ← (r2) − 1	Borrow		↕
DCRW	wa	2	13/17	(FFH, wa) ← (FFH, wa) − 1	Borrow		↕
INX	rp	1	7/9	(rp)←(rp) + 1			
DCX	rp	1	7/9	(rp)←(rp) − 1			
Miscellaneous							
DAA		1	4/6	Decimal adjust accumulator		↕	↕
STC		2	8/12	(CY) ← 1		1	
CLC		2	8/12	(CY) ← 0		0	
Rotate and Shift							
RLD		2	17/21	Rotate left digit			
RRD		2	17/21	Rotate right digit			
RAL		2	8/12	$(A_{m+1}) \leftarrow (A_m)$, $(A_0) \leftarrow$ (CY), (CY) ← (A_7)		↕	
RAR		2	8/12	$(A_{m-1}) \leftarrow (A_m)$, $(A_7) \leftarrow$ (CY), (CY) ← (A_0)		↕	
Jump							
JMP	word	3	10/16	(PC) ← word			
JB		1	4/6	$(PC_H) \leftarrow$ (B), $(PC_L) \leftarrow$ (C)			
JR	word	1	10/12	(PC) ← (PC) + 1 + jdisp1			
JRE	word	2	13/17	(PC) ← (PC) + 2 + jdisp			

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Instruction Set

Mnemonic	Operand	Bytes	*Clocks	Operation	Skip Condition	Flags CY	Flags Z
Call							
CALL	word	3	16/22	$((SP)-1) \leftarrow ((PC)+3)_H$, $((SP)-2) \leftarrow ((PC)+3)_L$, $(PC) \leftarrow$ word			
CALF	word	2	13/17	$((SP)-1) \leftarrow ((PC)+2)_H$, $((SP)-2) \leftarrow ((PC)+2)_L$, $(PC_{15}\text{-}PC_{11}) \leftarrow 00001$, $(PC_{10}\text{-}PC_0) \leftarrow$fa			
CALT	word	1	19/21	$((SP)-1) \leftarrow ((PC)+1)_H$, $((SP)-2) \leftarrow ((PC)+1)_L$, $(PC_L) \leftarrow (128+2ta)$, $(PC_H) \leftarrow (129+2ta)$			
Return							
RET		1	10/12	$(PC_L) \leftarrow ((SP))$, $(PC_H) \leftarrow ((SP)+1)$, $(SP) \leftarrow (SP)+2$			
RETS		1	10+n/12+n	$(PC_L) \leftarrow ((SP))$, $(PC_H) \leftarrow ((SP)+1)$, $(SP) \leftarrow (SP)+2$, $(PC) \leftarrow (PC)+n$			
RETI		1	13/15	$(PC_L) \leftarrow ((SP))$, $(PC_H) \leftarrow ((SP)+1)$, $(PSW) \leftarrow ((SP)+2)$, $(SP) \leftarrow (SP)+3$			
Skip							
SKNC		2	8/12	Skip if no carry	CY = 0		
SKNZ		2	8/12	Skip if co zero	Z = 0		
SKNIT	f	2	8/12	Skip if no INT X otherwise reset INT X	f = 0		
CPU Control							
NOP		1	4/6	No operation			
EI		2	8/12	Enable interrupt			
DI		2	8/12	Disable interrupt			
Serial Port Control							
SIO		1	4/6	Start (trigger) serial I/O			
STM		1	4/6	start timer			
Port E Control							
PEX		2	11/15	$(PE_{15}\text{-}PE_8) \leftarrow (B)$, $(PE_7\text{-}PE_0) \leftarrow (C)$			
PER		2	8/12	Port E AB mode			

Program Status Word (PSW) Operation

Operation					D_6	D_5	D_4	D_3	D_2	D_0
Reg. Memory		**Immediate**		**Skip**	**Z**	**SK**	**HC**	**L1**	**L0**	**CY**
ADD ADC SUB SBB	ADDX ADCX SUBX SBBX	ADI ACI SUI SBI			↕	0	↕	0	0	↕
ANA ORA XRA	ANAX ORAX XRAX	ANI ORI XRI	ANIW ORIW		↕	0	•	0	0	•
ADDNC SUBNB GTA LTA	ADDNCX SUBNBX GTAX LTAX	ADINC SUINB GTI LTI	 GTIW LTIW		↕	↕	↕	0	0	↕
	ONAX OFFAX	ONI OFFI	ONIW OFFIW		↕	↕	•	0	0	•
NEA EQA	NEAX EQAX	NEI EQI	NEIW EQIW		↕	↕	↕	0	0	↕
INR DCR	INRW DCRW				↕	↕	↕	0	0	•
DAA					↕	0	↕	0	0	↕
RLL, RLR					•	0	•	0	0	↕
RLD-RRD					•	0	•	0	0	•
STC					•	0	•	0	0	1
CLC					•	0	•	0	0	0
		MVI A, byte			•	0	•	1	0	•
		MVI L, byte LXI H, word			•	0	•	0	1	•
				SKNC SKNZ SKNIT	•	↕	•	0	0	•
				RETS	•	1	•	0	0	•
All other instructions					•	0	•	0	0	•

Flag Symbols:

↕ Flag affected according to result of operation.
1 Flag set
0 Flag reset
• Flag not affected.

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